(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 391 672 A1**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: **90303571.5**

(51) Int. Cl.5: **G05F 3/20**

(22) Date of filing: **03.04.90**

(30) Priority: **07.04.89 US 335420**

(43) Date of publication of application:
**10.10.90 Bulletin 90/41**

(84) Designated Contracting States:
**AT BE CH DE DK ES FR GB GR IT LI LU NL SE**

(71) Applicant: **HONEYWELL INC.**
**Honeywell Plaza**
**Minneapolis Minnesota 55408(US)**

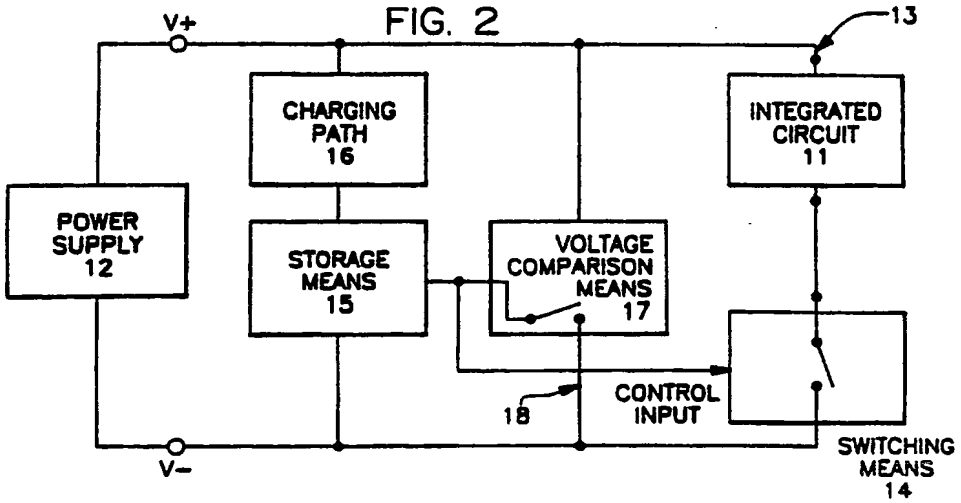
(72) Inventor: **Ratz, James W.**
**9124 Toledo Road**
**Bloomington, Minnesota 55437(US)**

(74) Representative: **Fox-Male, Nicholas Vincent Humbert**
**Honeywell Control Systems Ltd Charles Square**
**Bracknell Berkshire RG12 1FR(GB)**

## (54) Circuit to automatically power down a CMOS device which is latched up.

(57) An integrated circuit protection device for resetting an integrated circuit (11) when latch-up occurs has switching means (14) connected in series with a current path (13) to selectively control the flow of current through the integrated circuit. Voltage comparison means (17) monitors changes in voltage which correspond to changes in the current flowing through the integrated circuit. The voltage comparison means operates cooperatively with storage means (15) to provide an output to control the switching means (14). When latch-up is detected, the output signal to the switching means causes it to restrict current flow through the integrated circuit.

FIG. 2




EP 0 391 672 A1

## BACKGROUND OF THE INVENTION

A common fault condition associated with CMOS microprocessors and other triple diffused integrated circuits is known as "latch-up". Latch-up occurs due to parasitic transistors which are inadvertently established in the substrate and well regions during the construction of integrated circuits. A pair of parasitic transistors can interact through the intrinsic resistances of the device and form a circuit which operates similar to an SCR.

During the normal operating conditions of the integrated circuit, the parasitic transistors are biased off and thus do not conduct substantial current. The parasitic "SCR" is never intentionally activated during the operation of the integrated circuit. If, however, a transient causes the base of either parasitic transistor to go high, current is allowed to flow from a power supply through that transistor. The current flow causes a voltage drop across the inherent well resistance or substrate resistance which turns on the other corresponding transistor. Both transistors are consequently "latched" on and remain on until the voltage supplied by the power supply is removed or the current is limited such that the transistors are forced to turn off.

The current flowing when latch-up occurs is substantial and can render the entire integrated circuit inoperative and even cause thermal destruction. Thus, methods have been devised to reduce the possibility of latch-up. Both the layout and the process of manufacture of integrated circuits have been altered to reduce formation of the SCR-type circuits. However, these methods merely minimize the possibility of latch-up. Due to this limitation, it is often desirable to detect the occurrence of latch-up and reset the integrated circuit in the event that it does occur.

## SUMMARY OF THE INVENTION

In accordance, the present invention provides an integrated circuit protection device for resetting an integrated circuit when latch-up occurs. A switching means is connected in series with a current path to selectively control the flow of current through the integrated circuit. A voltage comparison means monitors changes in voltage which correspond to changes in the current flowing through the integrated circuit. The voltage comparison means operates cooperatively with a storage means to provide an output signal which controls the switching means. When latch-up is detected, the output signal to the switching means causes it to restrict current flow through the integrated circuit.

## BRIEF DESCRIPTION OF THE DRAWING

The invention will be better understood from a reading of the following description in conjunction with the drawing in which:

Fig. 1 is a schematic diagram of the parasitic transistors which form an SCR-type circuit within an integrated circuit;

Fig. 2 is a block diagram of the present invention; and

Fig. 3 is a schematic diagram of the preferred embodiment of the present invention;

## DETAILED DESCRIPTION

Figure 1 shows a cross sectional view of a portion of an integrated circuit with a schematic diagram of the parasitic transistors forming an SCR circuit within that portion of the integrated circuit. A power supply which powers the integrated circuit is connected at terminals $V^+$ and $V^-$. When a transient causes the base of either parasitic transistor to go high, current will flow from $V^+$ through the transistors to $V^-$. The integrated circuit will consequently be latched-up. When the integrated circuit is latched-up, the current flowing through the integrated circuit from the power supply must be restricted in order to deactivate the internal SCR. This process is hereinafter referred to as "resetting" the integrated circuit from its latched-up state.

Referring to Figure 2, an integrated circuit 11 susceptible to being latched-up is connected to a power supply 12 through a power supply current path 13. A switching means 14 is connected in series with the power supply current path 13 to selectively control the flow of current through the integrated circuit 11.

During normal operation of the integrated circuit 11, a storage means 15 is energized or charged through the charging path 16, and accordingly, a signal is provided to the control input of the switching means 14. The signal at the control input correspondingly closes the switching means 14 to allow current to flow from the power supply 12 to the integrated circuit 11.

If the integrated circuit 11 goes into latch-up, a substantial increase in current drawn from the power supply 12 occurs. When this sudden increase in current demand of the integrated circuit 11 occurs, the voltage level supplied by the power supply 12

at $V^+$ decreases. This voltage drop is especially noticeable if the power supply has been designed to meet the current demand during normal operation and little more. Power supply output resistance (commonly known as source resistance) is a cause of this drop in voltage when current output increases.

A voltage comparison means 17 is connected to the current path 13 and to the storage means 15. The voltage comparison means 17 monitors the sudden increase in current flow by measuring a corresponding drop in the voltage level at the terminal $V^+$. If the integrated circuit 11 goes into latch-up, a drop in the voltage at $V^+$ will be detected by the voltage comparison means 17. When latch-up is detected, the voltage comparison means 17 will provide for or activate a discharging current path 18 through which current can flow to discharge or deenergize the storage means 15. When the storage means 15 discharges, the signal applied at the control input of the switching means 14 will cause the switching means 14 to open and restrict current flow through the integrated circuit 11. The integrated circuit 11 will consequently be reset since the internal SCR-type circuit activated in the integrated circuit 11 is starved of current and hence will turn off. The time following latch-up detection during which the switching means 14 interrupts current flow is adjustable and controllable depending upon the characteristics of storage means 15 and charging path 16.

After latch-up is detected and current is restricted from flowing through the integrated circuit 11 by switching means 14, the discharging current path 18 is no longer provided for or activated by voltage comparison means 17. Consequently, storage means 15 recharges or reenergizes and the signal provided to the control input of switching means 14 causes the switching means 14 to again allow current flow through the integrated circuit 11.

Next, referring to Figure 3, there is shown a specific schematic diagram of a circuit which corresponds to the block diagram of Figure 2. The circuit is connected to control the current flowing through an integrated circuit 11. Specifically, the circuit interrupts the power supply current path 23 through the integrated circuit 11 when the supply voltage drops a certain amount in a given time interval.

A field effect transistor (FET) 22 is connected in series from drain to source in the power supply current path 23. The FET 22 is an N channel enhancement type with a threshold voltage of approximately 1.5 volts in this particular application.

During normal operation of the integrated circuit 11, the supply voltage at $V^+$ is at a certain voltage level and stable. During this time, the same voltage level is present across capacitor 24 due to charging current through resistor 25. Negligible current flows through the gate of the unijunction transistor 26 and hence the voltage at the gate is nearly equal to the voltage level at $V^+$. The unijunction transistor 26 is consequently biased off since its gate voltage is equal or substantially equal to the voltage level at its anode established across capacitor 24.

When the unijunction transistor 26 is biased off, current is not allowed to flow from the anode to the cathode of the device, and consequently, base current is not available to turn on bipolar transistor 27. Hence, during normal operation of the integrated circuit 11, the bipolar transistor 27 is biased off.

When the bipolar transistor 27 is off, very little current flows through its collector to emitter. Hence, and because negligible gate current flows through FET 22, the voltage drop across the resistor 28 is small. Consequently, the voltage at the gate of FET 22 is substantially equal to the voltage charged across the capacitor 24. This gate voltage is sufficiently high to bias the FET 22 on which therefore allows current to flow through the integrated circuit 11 supply terminals, maintaining normal operation.

It should be noted that during this period of normal integrated circuit operation, the power drawn by the circuit of the present invention is quite insubstantial. This characteristic is particularly important in applications where a source of power for the circuit is a battery.

A drop in the voltage at $V^+$ when latch-up occurs causes a corresponding drop in voltage at the gate of the unijunction transistor 26. Since the time constant of the RC network comprising capacitor 24 and resistor 25 is relatively slow (.33 sec. in this application), and the voltage across the capacitor 24 does not change instantaneously, the drop in the initial supply voltage level is represented across the anode and gate of the unijunction transistor 26. If the drop in $V^+$ is sufficiently large to cause the gate voltage to drop below the anode voltage by approximately .6 volts, the unijunction transistor 26 will trigger on.

When the unijunction transistor 26 turns on, current is allowed to flow from its anode to its cathode. Consequently, and due to the voltage level charged across the capacitor 24, the bipolar transistor 27 is biased on. This in turn causes the gate voltage of the FET 22 to drop below its threshold voltage and turn the FET 22 off. In addition, discharge current is allowed to flow from the capacitor 24, through resistor 28, and through the collector to emitter of transistor 27 to $V^-$. Since the time constant established by this discharging current path is relatively fast, the capacitor 24 discharges quickly.

It is important to note that the capacitor 24 will not recharge quickly since the time constant established by the resistor 25 connecting the capacitor to the power supply at $V^+$ is relatively slow. It is also important to note that once the unijunction transistor 26 has been turned on, it does not turn back off until the current flowing from its anode to cathode falls below the valley current level of the device. In addition, the current flowing through the resistor 25 is sufficiently less than the valley current level of the unijunction transistor 26 such that current flowing from the supply $V^+$ cannot maintain the on state of the unijunction transistor 26.

When the FET 22 turns off, current is not allowed to flow through the power supply current path 23 to the power supply terminals of the integrated circuit 11. This consequently resets latch-up and decreases the current demand which will correspondingly cause an increase in the voltage level at $V^+$.

After the FET 22 turns off, the voltage across capacitor 24 drops further as current continues to discharge through the bipolar transistor 27. When the capacity of the capacitor 24 decreases to a certain point, the unijunction transistor 26 and the bipolar transistor 27 will turn off.

When the bipolar transistor 27 turns off, the discharging current path for the capacitor 24 to discharge is not provided through the bipolar transistor 27. Consequently, the capacitor voltage rises due to charging current through the resistor 25. Again, it is pointed out that the time constant provided by this RC network is relatively slow. The capacitor 24 will eventually charge to its capacity, and the voltage across it will be equal to the supply voltage at $V^+$.

As the voltage across the capacitor 24 rises, the FET 22 will turn back on when the voltage at its gate rises above its threshold voltage of approximately 1.5 volts. When this occurs, current to supply the integrated circuit 11 with power is again allowed to flow through the power supply current path 23.

The time during which current is not allowed to flow allows the latched-up integrated circuit to reset. When this occurs, the parasitic transistors forming the SCR-type circuit within the integrated circuit 11 are forced to turn off. Hence, when current is allowed to flow after resetting the integrated circuit 11, it resumes in normal operation.

The amount of time during which the FET 22 is off and current flow through the integrated circuit 11 is restricted is determined by the RC time constant established by the resistor 25 and capacitor 24. Hence, by selecting different values of resistor 25 and capacitor 26, the amount of time during which current flow is restricted is adjustable and controllable. For different microprocessors or other CMOS devices, it may be desirable to vary the time constant in order to achieve optimum results.

It is also important to note that the delay time provided by the RC network during which current flow is impeded could be essential in assuring that the latch-up condition of the integrated circuit 11 will be reset. This could be of particular importance if parasitic capacitances within the device maintained sufficient capacity to keep on one of the parasitic transistors within the SCR-type circuit for a period of time.

Another feature of the present invention is the one-shot triggering of the circuit provided by the unijunction transistor 26 when latch-up is detected. Once the voltage at the gate of the unijunction transistor 26 falls below approximately 0.6 volts with respect to the anode, the device turns on. It will not turn back off if the voltage at its gate momentarily rises. Hence, the possibility of "chattering" of the circuit is eliminated. This is of particular importance if the same circuit is to be adapted for use with a variety of both microprocessors and power supplies.

Due to the arrangement of the storage means and the voltage comparison means comprising capacitor 24 and unijunction transistor 26 respectively, the latch-up detection circuit monitors sudden changes in current flow within a certain time interval, as opposed to merely monitoring when the current exceeds a certain level. As a result, the identical latch-up detection circuit can be used with different integrated circuits even though they each may have substantially unequal current demands during normal operation. Furthermore, gradual changes in current demand will not trigger the latch-up monitoring circuit.

It is apparent that an electromechanical relay or other switching means could be substituted in place of the field effect transistor. Additionally, the functions of the voltage comparison means and the storage means could be provided by a microprocessor or other circuitry.

In application where the power supply is capable of providing a substantially constant voltage level at $V^+$ as current varies, it may be required to increase the source resistance. Alternatively, an additional resistor could be connected in series with the power supply current path 23 such that the voltage comparison means would monitor the voltage drop occurring across it.

## Claims

1. A latch-up detection circuit for detecting latch-up of an integrated circuit (11) and for resetting the integrated circuit connected to a power

supply (12) through a power supply current path, the latch-up detection circuit characterised by:
a switching means (14) connected to the power supply current path, said switching means having a control input for selectivity restricting current flow through the power supply current path;
a storage means (15) electrically connected to the power supply current path and to said control input of said switching means; and
voltage comparison means (17) electrically connected to said storage means and to the power supply current path.

2. A latch-up detection circuit according to Claim 1 characterised in that said storage means (15) operates cooperatively with said voltage comparison means (17) for providing an output signal to said control input of said switching means.

3. A latch-up detection circuit according to Claim 1 or 2 characterised in that said storage means (15) comprises a capacitor.

4. A latch-up detection circuit according to Claim 3 characterised in that said capacitor (15) is connected to the power supply current path by a charging current path comprising a resistor.

5. A latch-up detection circuit according to any preceding Claim characterised in that said voltage comparison means (17) provides for a discharging current path connected to said storage means (15) for discharging said storage means when a voltage level on the power supply current path is below a certain threshold voltage with respect to a voltage level of said storage means.

6. A latch-up detection circuit according to my preceding Claim characterised in that said voltage comparison means (17) provides a discharging current path connected to said storage means (15) for discharging said storage means (15) when the integrated circuit (11) is latched-up.

7. A latch-up detection circuit according to any preceding Claim characterised in that said switching means (14) is connected in series with the current path.

8. A latch-up detection according to any preceding Claim characterised in that said switching means (14) comprises a relay.

9. A latch-up detection circuit according to any preceding Claim characterised in that said voltage comparison means (17) is connected to monitor a voltage across a resistor connected in the power supply current path.

10. A latch-up detection circuit according to any preceding Claim characterised in that said voltage comparison means (17) comprises a unijunction transistor.

11. A latch-up detection circuit according to Claim 10 characterised in that said unijunction transistor (17) is connected to detect a change in a voltage level on the power supply current path.

12. A latch-up detection circuit according to any preceding Claim characterised in that said switching means (14) comprises a field effect transistor (22).

13. A latch-up detection circuit according to any preceeding Claim, characterised in that said storage means (15) causes said switching means (14) to restrict the current flow through the power supply current path for a controlled period of time after latch-up is detected.

14. A latch-up detection circuit for detecting latch-up of an integrated circuit and for resetting the integrated circuit after latch-up occurs, the integrated circuit (11) connected to a power supply (12) through a power supply current path, the latch-up detection circuit comprising:
a switching means (14) connected to the power supply current path having a control input for selectively causing said switching means to operate in a first conductive state or a second conductive state;
a storage means (15) electrically connected to the power supply current path and to said control input of said switching means (14); and
a voltage comparison means (17) electrically connected to said storage means (15) and to the power supply current path, said voltage comparison means operating cooperatively with said storage means to provide a first signal to said control input of said switching means when the integrated circuit is latched-up, said first signal causing said switching means to operate in said first conductive state.

15. A latch-up detection circuit according to Claim 14 characterised in that said voltage comparison means (17) actuates said discharging current path for discharging said storage means (15) when the current flow through the power supply current path increases a certain amount in a given time interval.

16. A latch-up detection circuit according to Claim 15 characterised in that said voltage comparison means (17) actuates said discharging current path for discharging said storage means (15) when the current flow through the power supply current path increases a certain amount in a given time interval.

17. A latch-up detection circuit according to any of Claims 14 to 16 characterised in that said voltage comparison means (17) detects when an instantaneous voltage on the power supply current path decreases with respect to a stored voltage.

18. A latch-up detection circuit of said first conductive state has a lower conductivity than said second conductive state.

19. A latch-up detection circuit according to any of Claims 14 to 18 characterised in that said switching means operates in said first conductive

state for a period of time after said voltage comparison means detects latch-up.

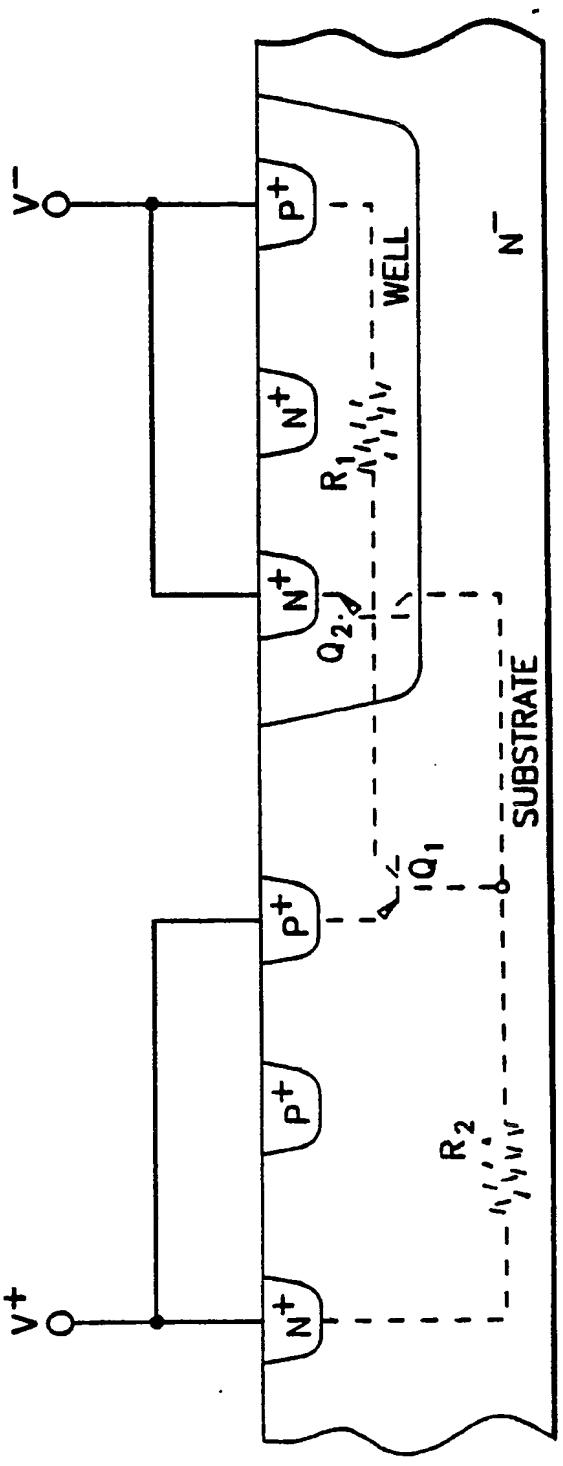



FIG. 1

FIG. 2

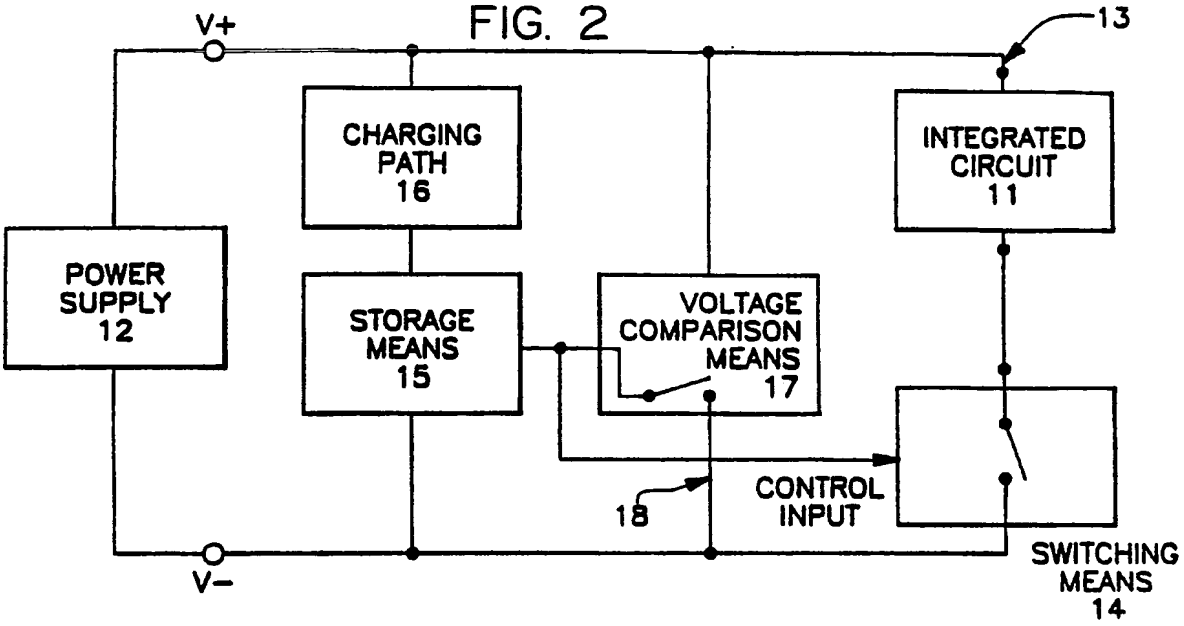
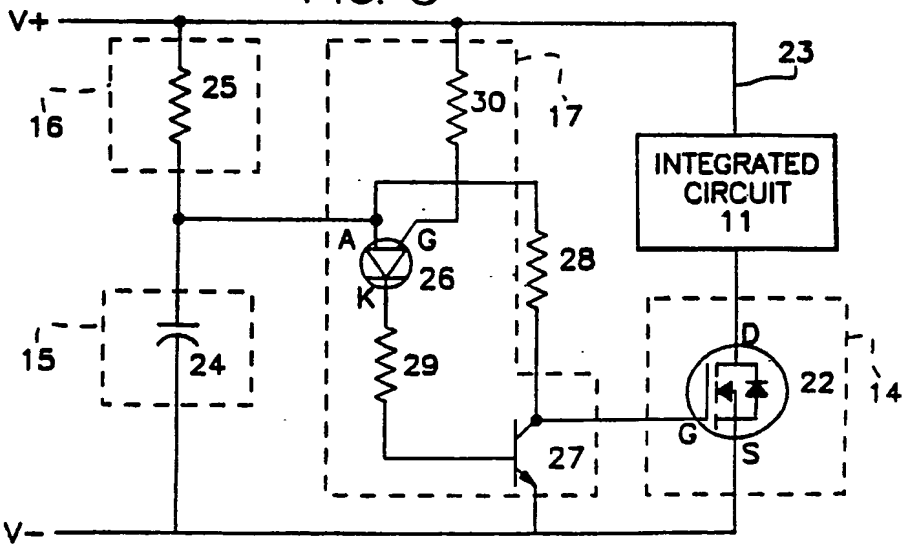

V+
13
CHARGING PATH 16
INTEGRATED CIRCUIT 11
POWER SUPPLY 12
STORAGE MEANS 15
VOLTAGE COMPARISON MEANS 17
18
CONTROL INPUT
V−
SWITCHING MEANS 14

FIG. 3


V+
16
25
30
17
23
INTEGRATED CIRCUIT 11
A
G
K
26
28
15
24
29
D
22
14
G
S
27
V−

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 90 30 3571

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.5) |
|---|---|---|---|
| X | US-A-4109161 (HIROSHI IIJIMA)<br>* the whole document * | 1, 2 | G05F3/20 |
| A | US-A-4260909 (A.C. DUMBRI, W. ROSENZWEIG)<br>* the whole document * | 1 | |
| A | EP-A-202074 (ADVANCED MICRO DEVICE)<br>* abstract; figure 3 * | 1 | |
| A | EP-A-175152 (LATTICE SEMICONDUCTOR)<br>* abstract; figures 1-7 * | 1 | |
| | | | TECHNICAL FIELDS SEARCHED (Int. Cl.5) |
| | | | G05F<br>H01L |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 20 JULY 1990 | ZAEGEL B.C. |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

1